Ruban S

Silicon Architect I

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Summary

I am a Silicon Architect at Google, currently working on Google's Tensor SoCs.

Prior to this, I was an Associate Engineer at MIPS Technologies, home to the MIPS ISA, where I worked in the Performance and Architecture Team. I have worked on performance modelling and correlation on Out-of-Order and In-Order Superscalar Multi-threaded CPUs based on the RISC-V ISA. I have worked with microbenchmarks like Dhrystone, Coremark, memcpy, daxpy, and also worked with larger benchmarks like SPECint.

I have a keen interest in learning about how computers work at a low-level, and seek to explore novel ideas in Computer Architecture, Compilers, Operating Systems and Networks. I'm also interested in reading and exploring technological innovations in retro computers and devices, and like to expand my knowledge in the field of semiconductors and VLSI.

Experience

Google | Silicon Architect I **Silicon Architect I: Nov 2024 – Present**

Part of the **gChips Team**. Working on **Google's Tensor SoCs** for Pixel mobiles.

MIPS Technologies | Associate Engineer **Associate Engineer: July 2023 – Nov 2024**
Intern: Jan 2023 – Jun 2023

Part of the **CPU Architecture and Performance Team**. Worked on the Out-of-Order **P8700** CPU, designed for ADAS applications, and currently working on the In-Order **I8500** CPU, designed as a DPU.

P8700 **Jan 2023 – Apr 2024**

- Played a significant role in **fine-tuning** the **branch predictor**, achieving a **98% accuracy** in Coremark
- Created and correlated **a performance model** for L1 and **L2 Prefetchers** using C++, and additionally tuned the L1 Prefetcher to provide an overall **12% increase in SPECint score**.
- **Diagnosed performance bottlenecks** in the RTL design using industry-standard **EDA tools**, focusing on the fetch and load/store units, and **proposed microarchitectural changes**.
- **Developed microbenchmarks** in **C** and **RISC-V assembly** to stress-test and **identify performance bottlenecks** in various CPU blocks, especially the floating-point and load/store units.

- **Identified compiler optimizations**, including compiler flags and instruction re-ordering heuristics, to generate optimized benchmark code, boosting overall performance.
- **Developed multiple visualization tools and scripts** in Python and Shell to **extract and analyze performance data** from RTL simulations and performance model runs.
- Enhanced **logging of performance-related information** from RTL simulations using Verilog.

I8500 **Apr 2024 – Nov 2024**

- Performed **correlation** on the **performance model** with **RTL design** by running microbenchmarks and **comparing performance statistics**.
- Identified compiler-level optimizations to generated optimized code.
- Enhanced tools and scripts in Python for performance data extraction and analysis.
- **Developed infrastructure** to **store** and maintain **performance workloads**.
- **Found performance bottlenecks** in the existing RTL design

Teaching Assistant for Computer Architecture | BITS Pilani **Semester I, 2022-23**

- Appointed as an Undergraduate Teaching Assistant for the course Computer Architecture (CS F342).
- Provided support to students during lab sessions.
- Set problems and solutions for lab exercises.
- Set the question (and solution) for the final lab exam.

Education

BITS Pilani Hyderabad Campus, B.E. Computer Science **2019 – 2023**

CGPA : 9.01

Bishop Cotton Boys' School, Science Stream **2017 – 2019**

Class 12 : 93.6 %

Bishop Cotton Boys' School, Bangalore **2005 – 2017**

Class 10 : 91.7 %

Projects

Cycle-Accurate RISC-V Performance Simulator

- This project is a cycle-accurate microarchitecture implementation of a simple in-order superscalar RISC-V CPU in C++.
- Built on top of Spike, an open-source RISC-V Instruction Simulator

Marr's Levels in A Microprocessor Model of The Brain | BITS Pilani **Aug – Dec' 2023**

- An attempt to reverse-engineer the 6502 microprocessor by comparing it's functionality to that of the human brain.
- Studied the 6502 at the transistor level of implementation.

Skills

- Computer Architecture
- Performance Modelling

Programming

- C (Experienced)
- C++ (Experienced)
- Python (Experienced)
- RISC-V Assembly (Experienced)
- Shell Scripting (Experienced)
- Verilog (Amateur)

Tools and Platforms

- Windows (Experienced)
- Linux (Experienced)
- Git (Skilled)
- Perforce (Experienced)
- Synopsys VCS (Experienced)
- Jira (Experienced)
- Jenkins (Intermediate)

Certifications

Oracle Cloud Infrastructure Foundations 2020 Certified Associate | Oracle

- The OCI Foundations certification is intended for individuals looking to demonstrate knowledge of public cloud services.

Languages

- English (Proficient)
- Hindi (Intermediate)
- Tamil (Intermediate)

Hobbies

- Sports – Basketball, Table Tennis
- Music fan – Progressive Rock
- Blogger – Computer Architecture